FPGA LOOKUP TABLE WITH TRANSMISSION GATE STRUCTURE FOR RELIABLE LOW-VOLTAGE OPERATION

ABSTRACT

A lookup table (LUT) for a field programmable gate array (FPGA) is designed to operate reliably at low voltage levels. The low-voltage LUT uses CMOS pass gates instead of unpaired N-channel transistors to select one memory cell output as the LUT output signal. Therefore, no voltage drop occurs across the pass gates. While this modification significantly increases the overall gate count of the LUT, this disadvantage can be mitigated by removing the half-latches required in current designs, and by removing initialization circuitry made unnecessary by the modification. Some embodiments include a decoder that decreases the number of pass gates between the memory cells and the output terminal, at the cost of an increased delay on the input paths that traverse the decoder.